



## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

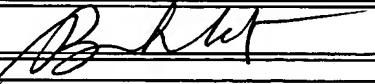
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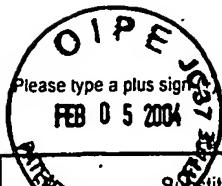
Stylesheet Version v18.0

Title of Invention	Method and apparatus for routing a set of nets									
Application Number:	10/066187									
Confirmation Number:	5277									
First Named Applicant:	Steven Teig									
Attorney Docket Number:	SPLX.P0133									
Art Unit:	2825									
Examiner:	Binh C. Tat									
Search string:	( 6155725 or 6166441 or 6175950 or 6209123 or 6216252 or 6230306 or 6247167 or 6253363 or 6260179 or 6289495 or 6292929 or 6301686 or 6324674 or 6327693 or 6327694 or 6330707 or 6378121 or 6385758 or 6401234 or 6405358 or 6407434 or 6412097 or 6412102 or 6463575 or 6473891 or 6519751 or 6526555 or 6543043 or 6557145 or 6567967 or 6586281 or 6665852 ).pn.									
US Patent Documents										
Note: Applicant is not required to submit a paper copy of cited US Patent Documents										
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass			
B1	1	6155725	2000-12-05	Scepanovic et al.						
B1	2	6166441	2000-12-26	Geryk						
B1	3	6175950	2001-01-16	Scepanovic et al.	B1					
B1	4	6209123	2001-03-27	Maziasz et al.	B1					
B1	5	6216252	2001-04-10	Dangelo et al.	B1					
B1	6	6230306	2001-05-08	Raspopovic et al.	B1					
B1	7	6247167	2001-06-12	Raspopovic et al.	B1					
B1	8	6253363	2001-06-26	Gasanov et al.	B1					
B1	9	6260179	2001-07-10	Ohsawa et al.	B1					
B1	10	6289495	2001-09-11	Raspopovic et al.	B1					
B1	11	6292929	2001-09-18	Scepanovic et al.	B2					
B1	12	6301686	2001-10-09	Kikuchi et al.	B1					

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BT	14	6327693	2001-12-04	Cheng et al.	B1
BT	15	6327694	2001-12-04	Kanazawa	B1
BT	16	6330707	2001-12-11	Shinomiya et al.	B1
BT	17	6378121	2002-04-23	Hiraga	B2
BT	18	6385758	2002-05-07	Kikuchi et al.	B1
BT	19	6401234	2002-06-04	Alpert et al.	B1
BT	20	6405358	2002-06-11	Nuber	B1
BT	21	6407434	2002-06-18	Rostoker et al.	B1
BT	22	6412097	2002-06-25	Kikuchi et al.	B1
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BT	28	6543043	2003-04-01	Wang et al.	B1
BT	29	6557145	2003-04-29	Boyle et al.	B2
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BT	31	6586281	2003-07-01	Gabara et al.	B1
BT	32	6665852	2003-12-16	Xing et al.	B2

Signature

Examiner Name	Date
	06/10/04



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/066,456
Sheet	1	of	2	Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
				Attorney Docket Number	SPLX.P0099

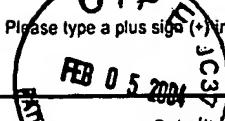
U.S. PATENT DOCUMENTS						
Examiner's Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (If known)			
KT	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
	4.	4,703,435		10-27-1987	Darringer et al.	
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	10.	6,080,204		06-27-2000	Mendel	
	11.	6,311,317	B1	10-30-2001	Khoche et al.	
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	15.	6,446,240	B1	09-03-2002	Iyer et al.	
	16.	6,453,447	B1	09-17-2002	Gardner et al.	
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	18.	6,519,754	B1	02-11-2003	McElvain et al.	
	19.	6,519,609	B1	02-11-2003	Touzet	
	20.	6,539,536	B1	03-25-2003	Singh et al.	
DK	21.	6,543,037	B1	04-01-2003	Limqueco et al.	

Examiner Signature		Date Considered	06/10/04
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This collection of information is required by 37CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO  
**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	2	of	2	Application Number	10/066,456
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
				Attorney Docket Number	SPLX.P0099

**U.S. PATENT DOCUMENTS**

RJ	22.	6,546,541	B1	04-08-2003	Petranovic et al.	
BT	23.	6,618,835	B1	09-09-2003	Garlapati et al.	

**NON PATENT LITERATURE DOCUMENTS**

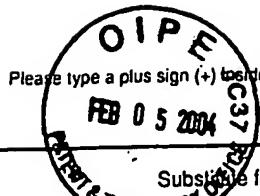
Examiner* Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>b</sup>
BT	24.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).	
BT	25.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vo.. 37, No. 11, pp. 291-292 (4 pages).	
BT	26.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargetting to Different CMOS Implementation Technologies", Proceedings of 2002 22 <sup>nd</sup> International Conference on Microelectronics", Vol. 2, 14 May 2000, pp. 703-706.	
BT	27.	Ruiz et al., " Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.	
BT	28.	Tamiya, Y., " Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.	

Examiner Signature		Date Considered	06/11/04
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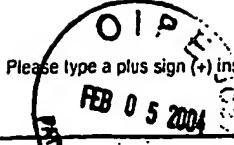
Substitute for form 1449A/PTO				Application Number	10/066,456
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
Sheet	1	of	2	Attorney Docket Number	SPLX.P0099

U.S. PATENT DOCUMENTS					
Examiner's Initials	Cite No. <sup>1</sup>	U.S. Patent Document Number	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
BT	1.	5,311,442	05-10-1994	Fukushima	
	2.	5,519,630	05-21-1996	Nishiyama et al.	
	3.	5,521,835	05-28-1996	Trimberger	
	4.	5,537,341	07-16-1996	Rose et al.	
	5.	5,610,829	03-11-1997	Trimberger	
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	10.	6,023,566	02-08-2000	Belkhale et al.	
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	16.	6,336,208	01-01-2002	Mohan et al	
	17.	6,470,478	B1 10-22-2002	Bargh et al.	
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	19.	6,496,972	B1 12-17-2002	Segal	
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BT	21.	6,574,779	B2 06-03-2003	Allen et al.	

Examiner Signature		Date Considered	06/18/04
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Sheet	2	of	2	Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
B T	22.	Crastes, M. et al., A technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 <sup>th</sup> ACM/IEEE, June 17-21, 1991, pp. 93-98.	
B T	23.	Devadas, S. et al., Synthesis and Optimization for Robustly Delay-fault Testable Combinational Logic Circuits, Design Automation Conference, 1990, 27 <sup>th</sup> ACM/IEEE, June 24-28, 1990, pp.221-227.	
B T	24.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 <sup>th</sup> Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.	

Examiner Signature		Date Considered	06/11/07/04
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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

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Sheet	1	of	2	Application Number	10/066,456
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
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## RELATED U.S. PATENT APPLICATIONS

Examiner <sup>*</sup> Initials	Cite No. <sup>1</sup>	U.S. Patent Application		Name of Patentee or Applicant of Cited Document	Date of Filing MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Serial Number				
BT	1.	10/062,017		Steven Teig & Asmus Hetzel	01-31-02	
	2.	10/061,459		Steven Teig & Asmuz Hetzel	01-31-02	
	3.	10/062,014		Steven Teig & Asmus Hetzel	01-31-02	
	4.	10/062,044		Steven Teig & Asmuz Hetzel	01-31-02	
	5.	10/066,264		Steven Teig & Asmus Hetzel	01-31-02	
	6.	10/066,188		Steven Teig & Asmus Hetzel	01-31-02	
	7.	10/062,992		Steven Teig & Asmuz Hetzel	01-31-02	
	8.	10/061,474		Steven Teig & Asmus Hetzel	01-31-02	
	9.	10/061,719		Steven Teig & Asmus Hetzel	01-31-02	
	10.	10/062,993		Steven Teig & Asmus Hetzel	01-31-02	
BT	11.	10/062,047		Steven Teig & Asmuz Hetzel	01-31-02	

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BT	12.	5,649,165		Jain et al.	07-15-97	
BT	13.	6,301,687	B1	Jain et al.	10-09-01	

Examiner Signature	<i>Bohles</i>	Date Considered	<i>06/10/04</i>
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Sheet	2	of	2	Attorney Docket Number	SPLX.P0099

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner's Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
BS	14.	D. Jongeneel, R. Olten, Y. Watanabe and R. K. Brayton, Area and Search Space Control for Technology Mapping, 37 <sup>th</sup> Design Automation Conference, 86-91, 2000.	
	15.	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.	
	16.	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.	
	17.	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between, Proceedings of the 27 <sup>th</sup> Design Automation Conference, 361-364, 1990.	
	18.	Kamal Chaudhary and Massoud Pedram, A Near Optimal Algorithm for Technology Mapping Minimizing Area under Delay Constraints, Proceedings of the 29 <sup>th</sup> Design Automation Conference, 492-498, 1992.	
	19.	Kurt Keutzer, DAGON: Technology Binding and Local Optimization by DAG Matching, Proceedings of the 24 <sup>th</sup> Design Automation Conference, 341-347, 1987	
	20.	Randal Bryant, Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams, CMU CS Tech Report CMU-CS-92-160.	
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Examiner Signature		Date Considered	06/15/04
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